What is Claimed is:

1. A duty cycle management method for limiting the transmission duty cycle of a transmitter of a wireless device whereby said transmitter transmits packets in the form of individual packets and/or packet bursts, said packet bursts comprising a predetermined maximum number of contiguous packets, said transmitter being operable over a duration measurable as a series of time windows whereby each said time window comprises a predetermined number of timeslots with each timeslot having a predetermined nominal duration, said transmitter being configured for transmitting a packet during one said timeslot and having an associated predetermined duty cycle limit for said transmitted packets, said method comprising limiting the number of packets transmitted during each time period defined by one time window or adjacent time windows, on a sliding basis, so as to limit the duty cycle of transmissions during successive adjacent time windows to said predetermined duty cycle limit, whereby the transmission of packets is delayed as needed to establish sufficient idle period(s) during said one time window or adjacent time windows to maintain said duty cycle within said duty cycle limit.

2. A method according to claim 1 comprising incrementing a counter by an amount of IC for each timeslot in which a packet is transmitted by said transmitter and decrementing said counter by an amount DC for each idle timeslot and delaying transmission of any further packet if said counter amount exceeds a maximum counter amount equal to said predetermined number of timeslots per time window, whereby the ratio of IC to DC is said duty cycle limit.

3. A method according to claim 2 including identifying prior to the transmission of a packet the applicable mode of transmission, being either individual packet or packet burst mode and, if said packet burst transmission mode is identified, determining whether the counter amount plus the number of packets in the identified packet burst times IC is equal to or greater than the maximum counter amount and, if it is

transmitting an individual packet only and if it isn't transmitting said packet burst.

4. A method according to claim 3 and including, where the duty cycle is such that transmission of a single packet burst within one time window would render said counter amount close or equal to said maximum counter amount, transmitting said burst packets only if said counter amount is zero and, if said counter amount has been zero for at least a number of timeslots equal to said predetermined number of timeslots per time window, incrementing said counter by IC or, if said counter amount has not been zero for at least a number of timeslots equal to said predetermined number of timeslots per time window, incrementing said counter by two times IC.

5. A method according to claim 3 including providing priority, for transmission, to a predetermined maximum number of acknowledgement packet(s) by permitting transmission of up to maximum number of acknowledgement packet(s) when said counter amount is equal to or greater than said maximum count number but less than a predetermined priority maximum count.

6. A computer-readable medium containing computer instructions executable by a controller in communication with a transmitter of a wireless device, wherein said transmitter is operable over a duration measurable as a series of time windows with each said time window comprising a predetermined number of timeslots, said instructions performing the steps of incrementing a counter by an amount of IC for each timeslot in which a packet is transmitted by said transmitter and decrementing said counter by an amount DC for each idle timeslot and delaying transmission of any further packet when said counter amount exceeds a maximum counter amount of said predetermined number of timeslots per time window, whereby the ratio of IC to DC is said duty cycle limit.

7. A computer-readable medium according to claim 6 wherein said instructions perform the steps of identifying prior to the transmission of a packet the applicable

mode of transmission, being either individual packet or packet burst mode, and if said packet burst transmission mode is identified, determining whether the counter amount plus the number of packets in the identified packet burst times IC is equal to or greater than said maximum counter amount and if it is transmitting an individual packet only and if it isn't transmitting said packet burst.

8. A computer-readable medium according to claim 7 wherein said instructions include, where the duty cycle is such that transmission of a single packet burst within one time window would render said counter amount close or equal to said maximum counter amount, performing the following steps:

(a) transmitting said burst packets only if said counter amount is zero; and,

(b) if said counter amount has been zero for at least a number of timeslots equal to said predetermined number of timeslots per time window, incrementing said counter by IC or, if said counter amount has not been zero for at least a number of timeslots equal to said predetermined number of timeslots per time window, incrementing said counter by two times IC.

9. A duty cycle management system for use in a wireless device, said wireless device comprising a transmitter for transmitting packets in the form of individual packets and/or packet bursts, said packet bursts comprising a predetermined maximum number of contiguous packets, said transmitter being operable over a duration measurable as a series of time windows with each said time window comprising a predetermined number of timeslots, each said timeslot having a predetermined nominal duration, said transmitter being configured for transmitting a packet during one said timeslot and having an associated predetermined duty cycle limit for said transmitted packets, said duty cycle management system comprising a controller and a storage medium containing instructions executable by said controller for limiting the number of packets transmitted during each time period defined by one time window or adjacent time windows, on a sliding basis, so as to limit the duty cycle of transmissions during successive adjacent time windows to said predetermined duty cycle limit, whereby the

transmission of packets is delayed as needed to establish sufficient idle period(s) during said one time window or adjacent time windows to maintain said duty cycle within said duty cycle limit.

10. A system according to claim 9 comprising a counter wherein said counter is incremented by an amount of IC for each timeslot in which a packet is transmitted by said transmitter and said counter is decremented by an amount DC for each idle timeslot, and transmission of any further packet is delayed when said counter amount exceeds a maximum counter amount equal to said predetermined number of timeslots per time window, wherein the ratio of IC to DC is said duty cycle limit.

11. A system according to claim 10 wherein the applicable mode of transmission, being either individual packet or packet burst mode, is identified prior to the transmission of a packet and, where said packet burst transmission mode is identified, if the counter amount plus the number of packets in the identified packet burst times IC is equal to or greater than the maximum counter amount, only an individual packet is transmitted and otherwise said packet burst is transmitted.

12. A system according to claim 11 wherein the duty cycle is such that transmission of a single packet burst within one time window would render the counter amount close or equal to said maximum counter amount and said burst packets are transmitted only if said counter amount is zero, said counter being incremented by IC if said counter amount has been zero for at least a number of timeslots equal to said predetermined number of timeslots per time window and said counter is incremented by two times IC if said counter amount has not been zero for at least a number of timeslots equal to said predetermined number of timeslots per time window.

13. A system according to claim 11 wherein said controller in combination with said instructions is configured for providing priority, for transmission, to a predetermined maximum number of acknowledgement packet(s) by permitting transmission of up to

maximum number of acknowledgement packet(s) when said counter amount is equal to or greater than IC/DC times said maximum number of packets per packet burst but less than a predetermined maximum count.